NIT-217

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

T. OHKAWA et al

Serial No. 09/639,753 Group Art Unit: 2635

Filed: August 15, 2000 Examiner: C. Yang

For: RFID (RADIO FREQUENCY IDENTIFICATION) AND IC CARD

APPEAL BRIEF

Board of Patent Appeals and Interferences
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450 June 3, 2005

Sir:

This appeal is taken from the final rejection of claims 1-12 set forth in the Final Office Action dated August 3, 2004 (Paper No. 12). In accordance with 37 CFR §41.37, the Appellants address the following items.

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REAL PARTY IN INTEREST

The real party in interest of this application is the assignee of record, Hitachi, Ltd.

RELATED APPEALS AND INTERFERENCES

It is believed that there are no related appeals or interferences that will directly affect, be directly affected by, or have a bearing on the Board's decision in this appeal.

STATUS OF CLAIMS

Claims 1-12 are pending. All of pending claims 1-12 have been finally rejected. Accordingly, the final rejection of claims 1-12 is being appealed.

STATUS OF AMENDMENTS

No amendments have been filed since the mailing of the Final Office Action.

SUMMARY OF CLAIMED SUBJECT MATTER

The present invention solves a need in the prior art for a radio-frequency identification device (RFID) of reduced complexity and cost, which is capable of receiving power and receiving and transmitting information on a contactless basis.

The prior art has known various techniques for receiving power and communicating with an external apparatus on a contactless basis, including a contactless IC card which receives an AC wave via an antenna coil, and then rectifying the AC wave and supplying the resulting DC power or signal to internal circuits. Typically, a power-on-reset circuit is provided for maximizing the working voltage margin, including a hysteresis circuit to smooth out dynamic load variations. In one prior art example, a dummy load corresponding to a CPU operation load is applied before release of power-on-resetting, and the dummy load is removed at the time of release of reset.

However, the dummy load must be redesigned according to design changes in load for communication and design changes in the antenna coil. Further, the dummy load must be set to have a value inclusive of upper limits of individual CPU differences, individual communication load differences, and impedance variations due to temperature variations, such that

the start-up receiving power level has been higher than the operation receiving power level. Moreover, the prior art circuit arrangement has been complex and expensive.

One prior attempt to address these problems has employed an intermittent load operation to provide a dynamic impedance variation. According to this technique, the reset release voltage must be set to a value corresponding to the sum of a working guarantee voltage and a drop-down voltage inclusive of the upper limit of individual communication load differences, including temperature-based impedance variations. The startup voltage margin, however, is narrowed by this technique. Further, this technique does not account for design changes in the communication load or the antenna coil.

In addition, while typically the AC wave received by the antenna coil is rectified and smoothed to provide a power source to internal elements of the RFID, and communication with an external apparatus is carried by varying the load on the RFID, there can be a large variation in the width of the power supply voltage, such that the power supply voltage must be monitored at all times to determine when it is within the working guarantee range of the device so that the reset state can be released. The hysteresis circuit configuration known to the art has been configured so that the reset voltage is

set at the working guarantee voltage, and the sum of the reset voltage and a voltage drop due to dynamic load variations is used as the reset release voltage. This condition has been a cause of reducing the working voltage margin of the device.

To address these and other problems of the prior art, the present invention provides an RFID whose inner elements or integrated circuit is put in an active state from a reset state (inactive state) when it is detected that the level of the DC voltage, attained by rectifying the AC wave induced on the antenna, is higher than the reset release voltage level, and maintains the integrated circuit at a low impedance state in reset. That is, the integrated circuit has two states of impedance (a high impedance state and a low impedance state), as opposed to the conventional RFID, which has a high impedance state that is maintained even in reset.

Further, according to the invention, the RFID uses a simple configuration for the power-on-reset circuit and obtains a maximum working voltage range, because the reset release voltage can be equal to, or nearly equal to, the reset voltage. See page 8, lines 3-8 of the specification, as well as page 13, lines 11-22 and page 14, lines 9-10 thereof.

Fig. 1 shows a generalized configuration of a contactless IC card that can be configured to incorporate the RFID

according to the present invention. Simply shown, an IC chip 2 is connected with an antenna coil 3 on an IC card 1.

Fig. 2 is a schematic drawing of circuit blocks that may form the contactless IC card 1 of Fig. 1. Power is received from an external apparatus (not shown) through the antenna coil 3. An AC wave received by the antenna coil 3 is converted into DC power through a rectifying/smoothing circuit 4 in the IC chip 2. Then, at a DC voltage level corresponding to an upper limit imposed by a limiter circuit 5 for overvoltage protection, the DC power is supplied to each internal circuit. The power-on-reset circuit 7 and circuit elements making up the data communication circuit 6 are improved according to the present invention.

When the DC voltage is higher than a threshold voltage level predetermined for the power-on-reset circuit 7, each element of the data communication circuit 6 is released from a reset state to enter an active state. The AC wave received by the antenna coil 3 is fed to a demodulator-clock generator circuit 61 of the data communication circuit 6, which then generates a clock signal for processor 8. Using the clock signal thus generated, a reset circuit 63 produces a reset signal for activating the processor 8.

Information from the external apparatus is received by the IC card 1 through phase modulation of an AC wave. The phase-modulated AC wave is demodulated by the demodulator-clock generator circuit 61, and demodulated information is supplied to the processor 8.

A carrier signal used for information transmission from the IC card one to the external apparatus is generated by a carrier signal generator circuit 62 which divides the frequency of the clock signal to a predetermined frequency. The carrier signal is phase-modulated with a data signal from the processor 8 by a modulator 64. FETs 9 and 10 are switched by an output of the modulator 64 to intermittently turn on-off resistors 11 and 12 disposed between the terminals of the antenna coil 3 and circuit ground, thereby producing impedance variation in the IC chip 2. In other words, by using the carrier signal phase-modulated with the data signal, the dynamic impedance variation is produced in the IC card 1. The external apparatus can then perform phase demodulation to obtain information from the signals output from the antenna coil 3.

Referring to Fig. 3, when a DC power supply voltage reaches a predetermined reset release voltage, a power-on-reset signal from the power-on-reset circuit 7 (connected to

the R (reset) terminal of flip-flop 64a) is made to have a low level, causing the flip-flop 64a to be put in the active state. The carrier generator circuit 62 is also made active to generate the carrier signal. The carrier signal thus generated is applied to a CLK (clock) terminal of the flip-flop 64a and an input terminal of an exclusive-OR circuit 64b. In Fig. 3, the other input of the exclusive-OR circuit 64b is connected with the Q (output) terminal of the flip-flop 64a and the output terminal of the exclusive-OR circuit 64b is connected to gate terminals of the FETs 9 and 10.

When an input to the CLK terminal is changed from low to high, the flip-flop 64a operates so that the level of the data signal from the processor 8 connected with the D (data) terminal is output through the Q terminal. Therefore, until a change occurs in the data signal, the Q terminal remains low and the carrier terminal is fed intact to the output terminal of the exclusive-OR circuit 64b. When the data signal is high, an inverted signal of the carrier signal is output through the output terminal of the exclusive-OR circuit 64b. Consequently, according to the level of the data signal, the modulator 64 acts to perform phase inversion in synchronization with the carrier signal.

As switching elements, FETs 9 and 10 turn on when there gate input levels are high, and turn off when their gate input levels are low. Thus, when FETs 9 and 10 turn on, the resistors 11 and 12 connected with the terminals of the antenna coil 3 are grounded, thereby rendering low the impedance state of the IC chip 2.

Fig. 4 shows a timing chart for the circuit elements discussed above. With additional reference to Fig. 5, the reset release voltage in the power-on-reset circuit 7 must be higher than the sum of a logic working guarantee voltage (a reset voltage after the start of circuit operation) and a drop-down voltage due to a load resistance for communication. The drop-down voltage is considered to be large enough to compensate for errors in fabrication of the communication load resistors and variations with temperature thereof. Thus, reset is released and the load for communication is intermittently applied to the antenna coil by appropriately switching FETs 9 and 10.

Turning to Figs. 6, 7, and 8, the disclosed embodiment improves upon the prior art by providing an inverter 64c between the Q terminal of flip-flop 64a and one input of the exclusive-OR circuit 64b. By this arrangement, the power-on-reset circuit can be provided so that the reset release

voltage is equal to the reset voltage after the start of the circuit operation. When the DC power voltage reaches a predetermined reset release voltage level, a power-on-reset signal from the power-on-reset circuit 7 is made low, causing the flip-flop 64a to be made active. The carrier generator 62 is also made active to generate the carrier signal. The carrier signal thus generated is applied to the CLK terminal of the flip-flop 64a and an input terminal of the exclusive-OR circuit 64b, as described above. However, the input terminal of the exclusive-OR circuit 64b receives the inverted output from the Q terminal of the flip-flop 64a, due to the inverter 64c. Thus, when the input to the CLK terminal of the flip-flop 64a is changed from low to high, the level of the data from the processor 8 is output through the Q terminal and inverted, whereby the carrier signal is output as is through the output terminal of the exclusive-OR 64b. Thus, according to the level of the data signal, the modulator 64 acts to perform phase inversion in synchronization with the carrier signal.

As before, the FETs 9 and 10 turn on when their gate input levels are high and off when low. When turned on, the resistors 11 and 12 are grounded to decrease the impedance in the IC chip 2.

With reference to the timing chart of Fig. 7, this embodiment provides a circuit arrangement in which the load for communication is applied to the antenna coil terminals at the time of resetting. Thus, the power-on-reset circuit does not require a hysteresis characteristic.

With further reference to Fig. 8, and in contrast with Fig. 5, the reset release voltage in the power-on-reset circuit is substantially equal to the logical working guarantee voltage (the reset voltage after the start of circuit operation). Therefore, there is substantially no adverse effect due to errors in fabrication of the communication load resistors, variation with temperature thereof, design modifications thereof, design modifications of the antenna coil, or impedance variations in the transmission system including the external apparatus. Thus, it is possible to ensure a maximum working voltage range for the IC.

In a further modification illustrated in Fig. 9, an OR circuit 64d is provided between the output of modulator 64 and the gate terminals of FETs 9 and 10. One input of the OR circuit 64d is the output of the modulator 64, and the other input is the power-on-reset signal supplied from the power-on-reset circuit 7.

In this embodiment, the output of the OR circuit 64d has a high level when the power-on-reset signal is high, regardless of the output level of the modulator 64. Thus, at the time of resetting, the resistors 11 and 12 are grounded to render low the impedance of the IC chip 2, and there is no need for a hysteresis characteristic for the power-on-circuit 7. Accordingly, a maximum voltage range can be ensured by establishing the reset level at the circuit working guarantee voltage.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Claims 1-2, 4-8, and 11 stand rejected under 35 U.S.C. §102(b) as being unpatentable over Hanaoka, et al., US 5,521,590 (Hanaoka).

B. Claim 3 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Hanaoka in view of Hirano, et al., US 6,246,624 (Hirano).

C. Claims 9-10 and 12 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Hanaoka in view of Beigel, US 5,973,598 (Beigel).

ARGUMENT

References Relied Upon by the Examiner

Hanaoka, et al., US 5,521,590 (Hanaoka)

Hirano, et al., US 6,246,624 (Hirano)

Beigel, US 5,973,598 (Beigel)

A. Claims 1-2, 4-8, and 11 stand rejected under 35 U.S.C. §102(b) as being unpatentable over Hanaoka, et al., US 5,521,590 (Hanaoka).

Claim 1

Independent Claim 1 features first means for releasing inner elements of a semiconductor device from a reset (inactive) state and putting the inner elements in an active state when a voltage attained by rectifying an AC wave received from an antenna is higher than a predetermined voltage value, wherein, in the reset state, the impedance of the semiconductor device is maintained at a low impedance state. This situation is illustrated, for example, in Fig. 7 of the present application. Note "R INPUT SIGNAL" of flip-flop 64a and the corresponding "SWITCHING BEHAVIOR OF FET 9, 10", which exhibits the ON state during the reset. As shown in Fig. 6, the ON state of FETs 9, 10 add resistors 11, 12

between coil 3 and ground, thereby lowering the impedance of the semiconductor device.

In contrast, Hanaoka discloses that the impedance is high in the case of the reset state, and low in the reset release state, the exact opposite of the presently claimed invention. The Hanaoka situation is illustrated in Fig. 4 of the present application. Note "R INPUT SIGNAL" and "SWITCHING BEHAVIOR OF FET 9, 10", referring to Fig. 2. Fig. 4 shows that the FETs 9, 10 are OFF during the reset period.

Further, it is clear from the details of Fig. 5 and Fig. 8 of the patent, that the data carrier 200 is in the reset state when the switch 15 is OFF. When the switch 15 is OFF, the voltage level of the data carrier 200 is fixed to VDD (High). Thus, the voltage input to the switch T1 is VDD (High) and not zero, so that T1 is opened (or "off").

The Appellants have carefully considered the Examiner's Response to Arguments, in the Final Office Action, addressing this matter. In reply, the Appellants note that the output of a circuit in a reset state need not necessarily be zero, as implied in the Examiner's Response. Rather, the output of the circuit in the reset state is determined by the actual circuit configuration. The suggestion that the transistor may float and cause Hanaoka's data carrier to act spuriously is not

precluded by the teachings of the patent, and the Examiner's suggested fix to prevent spurious output is likewise not disclosed in the patent. Moreover, the Appellants are not required to prove whether Hanaoka is operable or not operable, but can only truly respond to a prima facie case of obviousness, which is not made out by a mere suggestion that OUTDATA might be driven low during reset.

Furthermore, referring to Fig. 8, transistor T4 (switch 15) takes the ON state when a voltage V_{S1} exceeds a fixed voltage V_{ON}, such that electric power is supplied on the power source line V_{S2}. Immediately after the electric power is supplied on the power source line V_{S2}, the logic circuit of the data carrier main circuit 100 is controlled into an initial state by power-on reset circuit 14, and enters the standby state. Then, communication by modulation of alternating-current magnetic field can begin. The transistor T4 takes the OFF state when the voltage V_{S1} is less than a minimum operation voltage V_{OFF}. Therefore, supply of electric power on the power source line V_{S2} is interrupted when transistor T4 turns OFF, whereby the data carrier main circuit 100 does not operate (enters the inactive state).

As shown in Fig. 8, the data carrier main circuit 100 is always connected to the reference potential line V_{DD}, even when

switch 15 is open. On the other hand, when switch 15 (transistor T4) is open, there is no power supplied to line V_{S2}, so that the voltage of the output data OUTDATA is either (a) the voltage of the reference potential line V_{DD}, or (b) floating. The voltage of the output data OUTDATA in case (b) depends on the voltage immediately before the switch 15 is opened. Thus, it is not true that the voltage of the output data OUTDATA is always low when the data carrier main circuit 100 is in the reset, or inactive, state. Therefore, transistor T1 is not necessarily in the ON state when the data carrier main circuit 100 is inactive (that is, when switch 15 is open or transistor T4 is OFF).

In fact, it is more likely that the voltage of the output data OUTDATA, when the data carrier main circuit 100 is in the floating state, approaches the voltage V_{DD}, because a switching element having an infinitely large resistance would be required to control the modulator circuit 2 in the OFF state. Of course, a switching element having infinitely large resistance does not exist.

In summary, when switch 15 (transistor T4) of Hanaoka is open,

(a) in the case where the voltage of the output data OUTDATA is the voltage of the reference potential line V_{DD}, the

transistor T1 is in the OFF state and the impedance state seen from the coil 1 is maintained in the high state, or

b) in the case where the voltage of the output data OUTDATA is in the floating state, the ON/OFF state of transistor T1 becomes indefinite and the high/low impedance state seen from the coil 1 becomes indefinite. Therefore, Hanaoka cannot be said to maintain the impedance of the semiconductor device in the low impendence state when in the reset, or inactive, state. At the very least, one cannot say that Hanaoka teaches that the impedance is maintained low.

In order to support a rejection for anticipation under §102(b), the applied reference must teach, expressly or inherently, each limitation set forth in the rejected claims. Respectfully, the Appellants submit that claim 1 is patentably distinguishable from Hanaoka based, at least, on Hanaoka's lack of any teaching or suggestion to provide the claimed RFID with a semiconductor circuit device whose impedance is maintained at a low impedance state when the device is in the reset (inactive) state.

CLAIM 2

Claim 2 is dependent from claim 1, and thus inherits the patentability of claim 1. Note, further, that claim 2 recites

the characteristic shown in Fig. 8, in which the reset release voltage is substantially equal to the logic working guarantee voltage. Hanaoka is not seen to disclose or fairly suggest this limitation.

CLAIM 4

Independent Claim 4 recites similar language respecting the low impedance state of the semiconductor device during reset. Therefore, claim 4 is also patentable.

In addition, claim 4 recites that, when the DC voltage attained by rectifying the received AC wave is lower than a threshold level, the semiconductor circuit device is put in the reset state. By this limitation, the reset state is required when the threshold level is not exceeded. Hanaoka does not appear to make this requirement.

CLAIM 5

Independent Claim 5 also recites similar language respecting the maintaining of the low impedance state (of an "integrated circuit element"). Therefore, claim 5 is also patentable.

In addition, claim 5 requires the integrated circuit element of the RFID to have memory means, logic processing

means, and power-on-reset means for releasing the logic processing means from a reset state (defined as "an inactive state of the logic processing means") and putting the logic processing means in an active state. Further, claim 5 defines the threshold voltage level as it pertains to the voltage applied to the power-on-reset means, as opposed to the reset state defined for the logic processing means. Thus, the low impedance state is maintained when the voltage applied to the power-on-reset means is lower than the threshold level.

Hanaoka does not appear to teach that the reset state is defined for logic processing means, and that the low impedance state is maintained for the integrated circuit element (including logic processing means and power-on-reset means) when the voltage applied to the power-on-reset means is lower than the threshold level.

CLAIM 6

Independent Claim 6 recites similar language respecting the low impedance state of an integrated circuit element. Therefore, claim 6 is also patentable.

Further, claim 6 requires the integrated circuit element to have "communication means, a logic circuit and power-on-reset means for releasing said logic circuit from a reset

state which is an inactive state of said logic circuit and putting said logic circuit in an active state". Like claim 5, claim 6 defines the threshold voltage level as it pertains to the voltage applied to the power-on-reset means. Thus, the low impedance state is maintained when the voltage applied to the power-on-reset means is lower than the threshold level.

Thus, as Hanaoka does not appear to teach that the reset state is defined for logic processing means as defined in claim 5, Hanaoka also does not appear to teach that the reset state is defined for the logic circuit of claim 6, and that the low impedance state is maintained for the integrated circuit element (including the logic circuit and power-on-reset means) when the voltage applied to the power-on-reset means is lower than the threshold level.

CLAIM 7

Independent Claim 7 recites similar language respecting the low impedance state of the integrated circuit element set forth in claim 5. Therefore, claim 7 is also patentable. It is noted that claim 7 does not recite an antenna, as required by claim 5.

CLAIM 8

Independent Claim 8 recites similar language respecting the low impedance state of the integrated circuit element set forth in claim 6. Therefore, claim 8 is also patentable. It is noted that claim 8 does not recite an antenna, as required by claim 6.

CLAIM 11

Dependent Claim 11 is directed to an IC card having the RFID set forth in claim 1. Therefore, claim 11 is also patentable for the same reasons claim 1 is patentable, as argued above.

B. Claim 3 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Hanaoka in view of Hirano, et al., US 6,246,624 (Hirano).

CLAIM 3

Dependent Claim 3 is derived from claim 1 via claim 2. Thus, because Hirano does not disclose (and is not cited as disclosing) the feature of maintaining a semiconductor device at the low impedance state when the device is in the reset state, the combination of Hanaoka with Hirano cannot legally render obvious the invention claimed in claim 3.

C. Claims 9-10 and 12 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Hanaoka in view of Beigel, US 5,973,598 (Beigel).

CLAIM 9

Claim 9 is an independent claim limited by requiring that, when a voltage applied to power-on-reset means is below a threshold level, the integrated circuit element is maintained at a low state. Therefore, claim 9 is patentable for the same reason that claim 1 is patentable, as argued above.

Further, one of ordinary skill is not led to combine Beigel's teachings with those of Hanaoka. Beigel discloses a circuit 83 which is controlled by the count value of circuit 81 and is employed as a variable load on the coil 65 as set forth in col. 6, lines 26-62 of the reference. However, the count value is not defined when the DC voltage is supplied and no determination is made whether the impedance of the load is high or low. See, col. 9, lines 40-41 of the reference.

Therefore, it is hard to see how one of ordinary skill in the art would look to Beigel to modify Hanaoka to achieve the claimed invention, when it seems that neither reference addresses the issue of maintaining the integrated circuit

element at low impedance when the voltage applied to the power-on-reset means is lower than the threshold level. In turn, it is not seen how the Beigel structure constitutes the claimed function, when the reset state is released, of "repeating an operation that a terminal of a load resistor whose another terminal is connected with a terminal of a coil of said antenna is connected to ground potential through a switching element and an operation that said terminal of said load resistor is disconnected from said ground potential by said switching element."

CLAIM 10

Claim 10 is an independent claim limited by requiring that, when a voltage applied to power-on-reset means is below a threshold level, a terminal of a load resistor connected to the coil is grounded. Therefore, claim 10 is patentable for the same reason that claim 1 is patentable, as argued above. Further, the combinability or motivation to combine Beigel with Hanaoka is traversed as above.

In addition, the Appellants note that Beigel does not disclose that when a voltage is applied to the power-on-reset means that is lower than a threshold level, a terminal of the load resistor having another terminal connected with a

terminal of a coil of the antenna is connected to a ground potential through a switching element, as claimed. Therefore, even in combination with Hanaoka, the claims are not rendered obvious.

CLAIM 12

Dependent Claim 12 is directed to an IC card having the RFID set forth in claim 10. Therefore, claim 12 is also patentable for the same reasons claim 10 is patentable, as argued above.

CONCLUSION

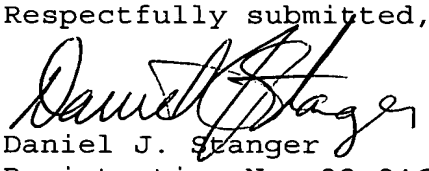
For the foregoing reasons, the Appellants respectfully submit that the rejection of the claims on appeal should be reversed and the application allowed.

FEES

A Credit Card Payment Form is enclosed for $2660, including $2160 for the five-month Extension of Time fee to render this Brief timely, and the $500 fee for filing a Brief in support of an appeal.

If any further fees are due in connection with the filing of this Appeal Brief, including any Extension of Time fees that are necessary, the Commissioner is hereby authorized to charge Deposit Account No. 50-1417.

Respectfully submitted,



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CLAIMS APPENDIX

1. An RFID comprising:

an antenna for receiving power to drive a semiconductor circuit device and for transmitting and receiving signals; and

first means for releasing inner elements of said semiconductor device from a reset state which is an inactive state of said inner elements and putting said inner elements in an active state upon detection of a condition that a voltage attained by rectifying an AC wave induced on said antenna is higher than a predetermined voltage level;

wherein, when said reset state is released, information can be transmitted from said antenna to an external apparatus according to signals which are generated in said semiconductor circuit device by controlling two states of impedance of said semiconductor circuit device which are a high impedance state and a low impedance state, and

wherein, in said reset state, said impedance is maintained at said low impedance state.

2. The RFID according to claim 1,

wherein a reset release voltage for releasing said inner elements from said reset state is substantially equal to a

logic working guarantee voltage of an IC that is part of said RFID.

3. The RFID according to claim 2,

wherein said reset release voltage for releasing said inner elements from said reset state is equal to a reset voltage for putting said inner elements in said inactive state at the start of logic working of the IC after releasing said reset state.

4. An RFID comprising:

an antenna; and

first means for releasing inner elements of said semiconductor device from a reset state which is an inactive state of said inner elements and putting said inner elements in an active state upon detection of a condition that a DC voltage attained by rectifying an AC wave induced on said antenna is higher than a threshold level;

wherein, when said reset state is released, signal transmission from said antenna to an external apparatus can be performed according to signals which are generated in said semiconductor circuit device by controlling two states of

impedance of said semiconductor circuit device which are a high impedance state and a low impedance state,

wherein, when said DC voltage is lower than said threshold level, said semiconductor circuit device is put in said reset state, and

wherein, in said reset state, said impedance is decreased to a low state.

5. An RFID comprising:

an integrated circuit element having memory means, logic processing means, and power-on-reset means for releasing said logic processing means from a reset state which is an inactive state of said logic processing means and putting said logic processing means in an active state; and

an antenna for receiving power and signals from an external apparatus and for supplying said power and signals to said memory means and logic processing means;

wherein, when a voltage applied to said power-on-reset means is lower than a threshold level, impedance of said integrated circuit element is maintained at a low state.

6. An RFID comprising:

an integrated circuit element having communication means, a logic circuit and power-on-reset means for releasing said logic circuit from a reset state which is an inactive state of said logic circuit and putting said logic circuit in an active state; and

an antenna for receiving power and signals from an external apparatus and for supplying said power and signals to said communication means and logic circuit;

wherein, when a voltage applied to said power-on-reset means is lower than a threshold level, impedance of said IC device is maintained at a low state, and

wherein, when a reset state is released, signal transmission from said antenna to said external apparatus is performed according to signals which are generated in said integrated circuit element by controlling a state of said impedance of said integrated circuit element.

7. An RFID comprising:

an integrated circuit element having memory means, logic processing means and power-on-reset means for releasing said logic processing means from a reset state which is an inactive state of said logic processing means and putting said logic circuit in an active state;

wherein, when a voltage applied to said power-on-reset means is lower than a threshold level, impedance of said integrated circuit element is maintained at a low state.

8. An RFID comprising:

an integrated circuit element having communication means, a logic circuit and power-on-reset means for releasing said logic circuit from a reset state which is an inactive state of said logic circuit and putting said logic circuit in an active state;

wherein, when a voltage applied to said power-on reset means is lower than a threshold level, impedance of said integrated circuit element is maintained at a low state, and

wherein, when a reset state is released, signal transmission to an external apparatus is performed according to signals which are generated in said integrated circuit element by controlling a state of said impedance of said integrated circuit element.

9. An RFID comprising:

an integrated circuit element having communication means, a logic circuit and power-on-reset means for releasing said logic circuit from a reset state which is an inactive state of

said logic circuit and putting said logic circuit in an active state; and

an antenna for receiving power and signals from an external apparatus and for supplying said power and signals to said communication means and logic circuit;

wherein, when a voltage applied to said power-on-reset means is lower than a threshold level, impedance of said integrated circuit element is maintained at a low state, and

wherein, when a reset state is released, signal transmission from said antenna to said external apparatus is performed according to signals which are generated in said integrated circuit element by repeating an operation that a terminal of a load resistor whose another terminal is connected with a terminal of a coil of said antenna is connected to ground potential through a switching element and an operation that said terminal of said load resistor is disconnected from said ground potential by said switching element.

10. An RFID comprising:

an integrated circuit element having communication means, a logic circuit and power-on-reset means for releasing said logic circuit from a reset state which is an inactive state of

said logic circuit and putting said logic circuit in an active state; and

an antenna for receiving power and signals from an external apparatus and for supplying said power and signals to said communication means and logic circuit;

wherein, when a voltage applied to said power-on-reset means is lower than a threshold level, a terminal of a load resistor whose another terminal is connected with a terminal of a coil of said antenna is connected to ground potential through a switching element.

11. An IC card which has the RFID according to claim 1.

12. An IC card which has the RFID according to claim 10.